Amendments to the Specification

Please amend the paragraph at page 5, lines 31-32 as follows:

FIG. 4 ~~is a flow chart representing a method of~~ shows an apparatus that ~~processing~~ processes an instruction in an instruction pipeline according to an illustrative embodiment of the present invention.

Please amend the paragraph at page 20, line 29 through page 21, line 8 as follows:

FIG. 4 shows ~~a flow chart representing a method of~~ an apparatus that ~~processing~~ processes an instruction in an instruction pipeline ~~within~~ with an interrupt verification support mechanism according to an illustrative embodiment of the present invention. As already described in detail the instructions to be performed by the computer system are processed in the processor by flowing through an instruction pipeline. In the instruction pipeline, the instructions are processed sequentially in several stages, i.e. an instruction fetch stage 1, an instruction decode stage 2, an instruction issue stage 3, an instruction execute stage 4 and a result write-back stage 5. Each stage 1 to 5 may have a different instruction in it. The instruction fetch comprises a program counter PC and is coupled to the first input of a ~~de-multiplexer~~ multiplexer 6 for transmitting actual instructions to the ~~de-multiplexer~~ multiplexer 6. The second input of the ~~de-multiplexer~~ multiplexer 6 is connected to an interrupt pseudo-instruction input. Via said second input of the ~~de-multiplexer~~ multiplexer 6 interrupt pseudo-instruction signals or external interrupt requests can be received.